A NEW GENERATION OF DATA AND CONTROL INTERFACES FOR DIGITAL DETECTORS

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Abstract: *The purpose of this project, started in 2002 with the support of a two year grant from the Agenzia Spaziale Italiana (ASI), was the development of a modular detector-controller and data-handler compatible with present industrial and consumer bus/interfaces, i.e., VME, CPCI and PCI. As a second, but no less important, instance the system here described has been developed as an upgrade for the out of date VME/transputer interfacing systems still in operation at various Italian astronomical sites and also as a platform for more complicated detection systems (NIR/MIR cameras or large detector mosaics) to be implemented in the future. As a consequence this paper is intentionally focused on the digital structure of the system (data-flow, controls and telemetry), being the usual analog electronics typically embedded on a classical detector controller (i.e. pulse and voltage adapters, amplifiers etc.). This paper is less concerned with the overall architecture, which is only marginally mentioned herein. Several implementations of this system are already in operation in different astronomical applications, some of them presented during this meeting.*

Key words: *Detectors, control systems, electronics.*

1. INTRODUCTION

It is from the advent of modern CCD area detectors (in the second half of seventies) that the need for flexible detector controllers has emerged. The life-time for such control systems is determined not only by the evolution of

J.E. Beletic et al.(eds.), Scientific Detectors for Astronomy 2005, 679-684.

detectors and by the technological evolution of electronic components (converters, gate-arrays, printed circuit technology, etc.), but also by the need to have better connectivity in terms of throughput and ease of system insertion inside computers and advanced data networks. Looking back, we can estimate that the life-time of a detector controller system is typically between 5 and 10 years before it is obsolete. This project, named VISIR-C (Visual Infrared Controller), belongs to the third and last generation of controllers constructed by the authors of this paper. This evolution spans 25 years activity beginning with the first generation of detector control systems created in order to support small and medium ground-based observatories [1] and a second generation of systems constructed to support the Galileo National Observatory [2].

2. SYSTEM REQUIREMENTS

As a direct result of previously made considerations and by comparison with the present advancements in the field of detector controllers we derived the following requirements for the VISIR-C project [3,4]:

1. Upgrades for the previous generation of transputer based VME/VSB boards ensuring compatibility with high level SW (table editors)
2. Compatibility with modern bus architecture, i.e., PCI, CPCI, VME and use of dedicated single-chip modern bus-adapters (AMCC chips in this case)
3. Use of host computer memory for data storage via PCI fast data transfers assuring an easy upgrade path
4. Use of fast throughput, full-duplex, data & controls link between host interface and remote electronics (1.2 Gbaud in the present case)
5. On board (host interface) generation of detector clock sequences and transmission through the fast control link
6. A simple expansion scheme for the controller adding boards to the system.

3. THE PMC/PCI CONTROLLER INTERFACE

In order to achieve a high level of compatibility with modern bus structures, the PCI bus model has been used as a base for reference due to its presence at the CPU board level, as well as in different 'industrial' structures like the VME bus and the CPCI. It was thus possible to cover a wide range of bus standards with the construction of the two basic detector host-adapters shown in Fig. 1:

- the PCI model, covering low-cost PC based systems, and
- the PMC model, covering more professional structures like CPCI and VME

Both systems are built around a standard AMCC PCI bus adapter and are served by a Motorola DSP53301 processor acting as a programmable clock sequencer. The processor is compatible with the existing off-line software for clock waveforms design and run-length encoding. Clocks produced by the DSP at a stable tick time of 50 nSec are serialized, sent to the remote controller board and de-serialized. The same is done for commands and operands, so that the remote electronics are completely passive and a unique system clock is used at 40 Mhz on the remote head.

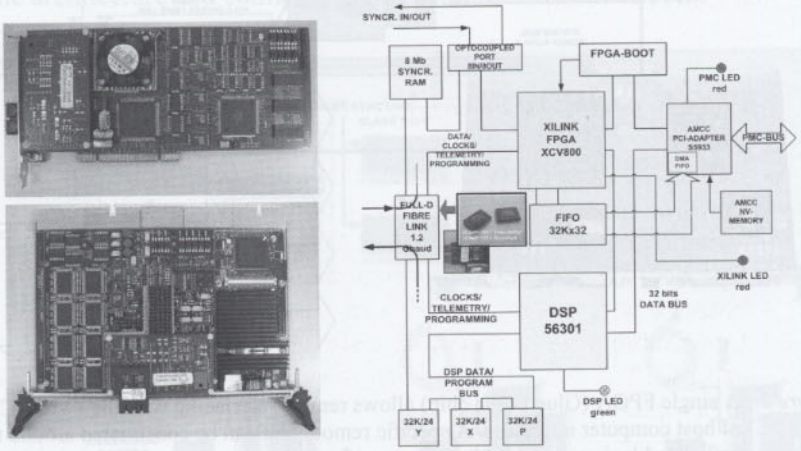

Figure 1. PCI and PMC interfaces. The PMC interface is based on a 'piggy-back' module (two PMC slots) typically mounted on the top of a CPU board (a Motorola CPV-5375 in the bottom picture) or in a PMC carrier board.

The more complex PMC module adds the presence of a large FPGA array, custom programmable from the host computer, to implement fast algorithms on the detector data flow.

The DSP 56301 and the FPGA have their own memory for data and programs; both can use the output channel to the remote unit for commands and readout sequences. This means that both can be used as clock-sequence generators. Conversely, the input fast channel for data can be used only by the FPGA. It is then possible to process data from the detector 'on the fly' using wired functions on the FPGA (co-adding, computation of event centroids, tracking of objects, etc.). The configuration of the FPGA can be changed so the controller interface can be remotely reprogrammed by downloading the micro-code into the dedicated memory from the host-

computer. Both boards are provided with an opto-coupled I/O port acting as a general services port or, if required, as a synchronization link for expanded systems (see Fig. 2).

4. THE REMOTE CONTROLLER INTERFACE

The remote unit is completely 'passive' in that no computing power has been implemented to reduce the clock/interference jitter on the system to a minimum.

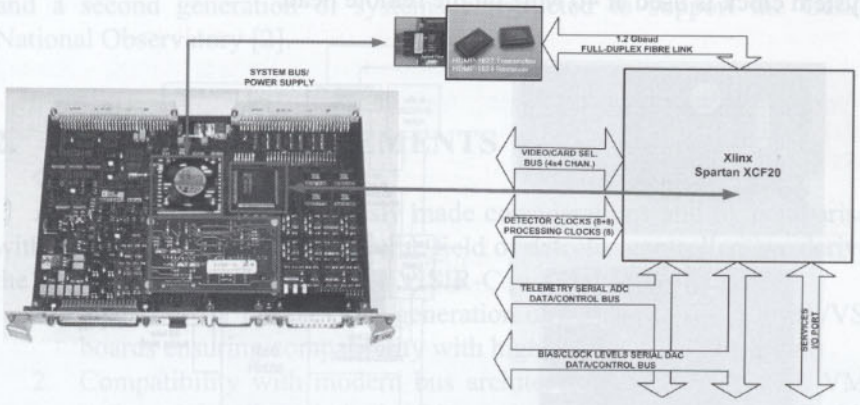

Figure 2. A single FPGA (Glue Logic chip) allows remote interfacing with the PMC/PCI set of host computer interfaces. A specific remote unit can be constructed around this embedded logic only by adding the specific analog functions required.

The central 'core' of this system is a Glue Logic chip that implements all the logic functions needed to drive a set of general-purpose analog boards customized for a given detector on an FPGA (Xilink Spartan series), i.e.:

- handling of a command/data/telemetry link to the PCI/PMC interface board,
- reformatting of detector clocks coming from the PCI/PMC interface board (8+8 programmable clock lines plus 8 pixel processing lines),
- handling of video channel data-flow (up to 4×4 16 bit channels),
- handling of serial DACs control lines for BIAS/CLOCK programming,
- handling of serial ADCs control lines for Telemetry acquisition, and
- handling of services (temperature and shutter control).

In our specific implementation, the basic remote unit has been mounted in a VME format board allowing compatibility with existing analog boards. Different implementations can be also imagined, for example a single,

compact, remote unit where the Glue Logic chip is directly embedded with the analog electronics.

The system is, in this way, customizable for a given application and/or detector focal plane, in that only the insertion of a specific set of analog boards is needed to configure it.

The requirement to expand the system with more complex control architecture (detector mosaics, multiple service cameras, etc.) has been satisfied by making use of host-computers. Figure 3 shows simple architecture based on PCI interface, where a common synchronization line driven by a master interface allows the building of a large system with no dedicated hardware other than the simple insertion of extra boards. The same architecture and configuration is valid for PMC interfaces.

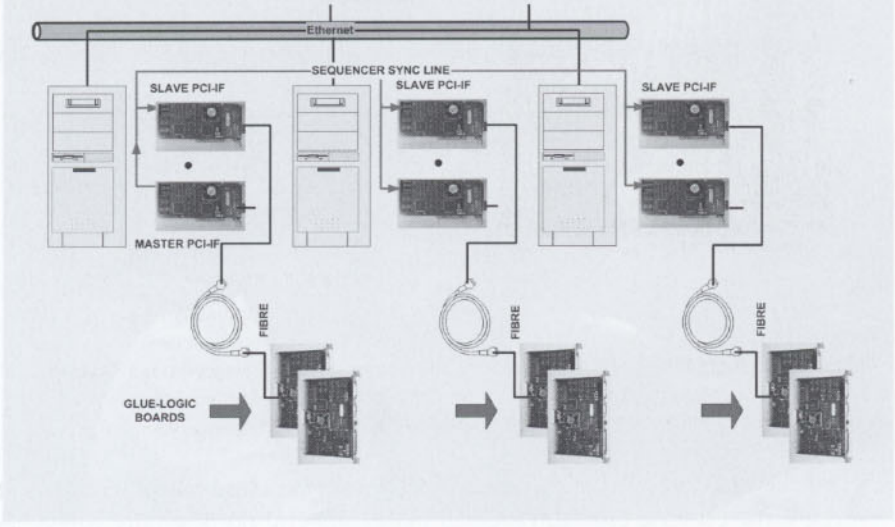

Figure 3. Expansion tree for the system based on a common synchronization line handled by a master host-computer interface.

5. CONCLUSIONS

A modular, general purpose detector control system has been studied, developed and tested. The system allows the handling of a variety of image detector configurations based on contemporary dominant technologies (CCD and CMOS multiplexer readout). The hardware can be remotely controlled, reconfigured, and asynchronous telemetry on every detector-crucial parameter captured. The system is compatible with a wide range of PCI, CPCI and VME host computer interfaces and it can be easily expanded inside this ambient to complex configurations.

6. REFERENCES

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Fernando Pedichini and Roberto Speziali holding their breath and eating pizza at the the same time.