The new generation CCD controller: first results

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Abstract: The new generation CCD controller, developed by the Italian Detector Working Group (DWG), is an improvement of the CCD controller in use at TNG. A new interface with the host computer, based on a high-speed link and PCI board, able to sustain high data transfer rate has been designed and built. The sequencer has been modified in order to improve high-speed clocks and different reading modes. A new analogue board based on a fast ADC's and new signal processing has been designed. The board is able to process four channels simultaneously allowing high acquisition rates. Preliminary tests demonstrating the improved performances of the controller are shown.

Key words: CCD, CCD controller

1. CCD CONTROLLER IMPROVEMENTS

The new generation CCD controller is an evolution of the controller in use at the TNG and at the local Italian telescopes. The same philosophy and the technological improvements guarantee an increase in performance and a full compatibility with the previous version. The change involved the host interface, the communication link, the sequencer, the bias generator, the clock generator, the preamplifier and the signal processing. In *Table 1* the main differences between the two controllers are shown.

The mains differences consist of a change in the architecture of the system. Basically the systems can be divided in two parts: the first next to the control computer (local), the other one next to the detector (remote). In the new CCD controller the preamplifier is integrated in the analogue board

that is mounted next to the detector and the sequence generation is located in the host computer, far from the detector. This is possible thanks to the capability of the high speed links to serialize and deserialize the sequence with a resolution of 50 ns.

This guarantees a high performance in terms of noise immunity.

Table 1. Main differences between the two controllers

CCDC MODEL	TNG CCDC-I 1994	TNG CCDC-II 2000
SEQUENCER	DSP 56001	DSP 56301
	RESOL.: 100 n Sec	**RESOL.: 50 n Sec**
DATA LINK	FIBER TRANSPUTER	FIBER GIGALINK
	LINK 20 M baud	**1.2 G baud**
CLOCK	LOCAL	HOST
DATA HANDLING	TRANSPUTER	HOST PROCESSOR
CHANNELS (16 bit ADC)	4 X 2 boards	4 X 8 boards
ADC speed	10 µ Sec	**2 µ Sec**
PIXEL PROCESSING	CORRELATED DUAL SLOPE	**CORRELATED DUAL SAMPLING SINGLE SAMPLING**
PROGRAMMABLE BIASES	8 (14 bit DAC) X 2 boards	16 (14 bit DAC) X 8 boards
PROGRAMMABLE CLOCKS	8 (8 bit DAC) X 2 boards	8+8+8 (10 bit DAC)
ADJ. OFF-SET	ONLY OUT-OFF/SET	IN and OUT OFF/SET
PROGRAMABLE GAIN	NO	15, 75, 150
PROGRAMABLE FILTER	NO	NONE, 234 KHz, 3.4 MHz
AMPLIFIER NOISE	4.5 µV (OPA627 @ 1Mhz, 10K)	1+2 µV (AD797 @ 1Mhz, 10K)
READOUT TIME	17 µSEC/PIXEL	2.7 µSEC/PIXEL

1.1 Host interface and communication link

The new host interface is a PCI based board, equipped with a full-duplex optical link, working at 1.2 G bauds. It allows the data and telemetry communication (remote to local) and command and clock sending (local to remote). The communication with high-level languages is guaranteed by low level drivers (Windows NT, 2000 and XP) and a DLL.

The architecture evolution of the new CCD controller respect to the old version is shown in figure *Figure 1*. Thanks to high speed link the phases are generated in the host computer and are rebuilt by remote. All the TTL signals, including the clock signals are generated on

the PCI board (far from the CCD head) while the analogue circuits are next to the CCD head. This guarantees a high noise immunity

1.2 Sequencer

The sequencer board mounts a MOTOROLA DSP 56301 and allows a minimum tick of 50 ns (with the previous controller it was 100 ns).

This solution guarantees the full compatibility with already developed software for sequence generation (Waveform Editor). Moreover, the clock levels are generated in this board (in the previous version it was generated in the analogue board). In this way a possible cause of cross talk is decreased.

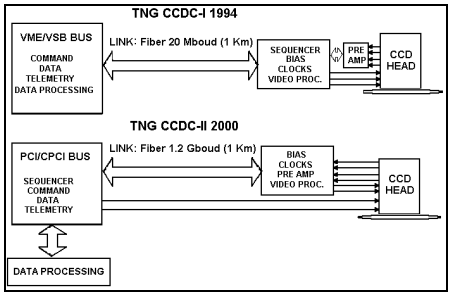

Figure 1. Block Diagram of the two CCD controller

1.3 Analogue board

The preamplifier (see figure 2) is based on the low noise Operational Amplifier AD 797. The configuration makes four gain selection, band pass filter selection and the input offset programmability possible.

The Signal Processing (see figure 3) is carried out by using the "Correlated Dual Sampling" technique (Single sampling is also allowed). The output offset can be adjusted through the 14-bit D/A Converter and the A/D Converter has 16 bits of resolution and a conversion time of 2 μs.

In summary, the analogue board allows three selectable input gains and three selectable bandwidths to work at different readout speed, the possibility to program the offsets before and after the CDS stage, to adapt the signal to the A/D converter and the choice of different reference for the dummy input. The bias generator allows 16 programmable bias voltages with different ranges, divided in four group. The ranges of voltages are: 15/30, 5/15, -5/5 and –10/10 volts.

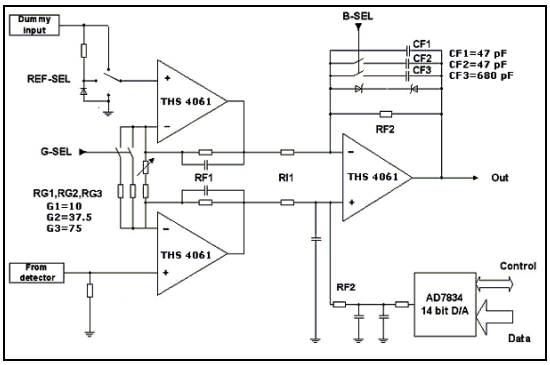

Figure 2. Preamplifier (one channel)

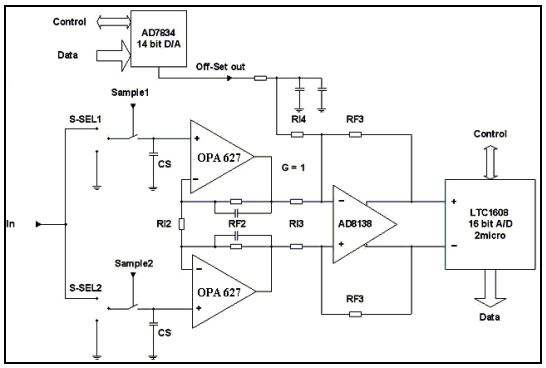

Figure 3. Signal Processing (one channel)

2. RESULTS

The new generation CCD controller lives up to expectations. The data acquisition rate is increased, the reliability is high and the readout noise is acceptable. The typical readout noise at different gain is showed in *Table 2*.

Table 2. Readout noise at different gains

GAIN	NOISE (DN)	NOISE (e^-) for sens. 3µV/ e^-
20	3	4.45 e^- r.m.s.
75	4	1.36 e^- r.m.s.
150	4.5	0.76 e^- r.m.s.