

CCD CAMERAS FOR THE ITALIAN NATIONAL TELESCOPE GALILEO

F. Bortoletto, C. Bonoli, M. D'Alessandro, D. Fantinel,
G. Farisato

Osservatorio Astronomico di Padova Vicolo dell'Osservatorio, 5, I - 35131 Padova (Italy)

G. Bonanno, P. Bruno, R. Cosentino

Osservatorio Astrofisico di Catania Viale A. Doria, 6, I - 95125 Catania (Italy)

G. Bregoli

Osservatorio Astronomico di Bologna, Via Zamboni, 33, I - 40126 Bologna (Italy)

M. Comari

Osservatorio Astronomico di Trieste, Via G.B. Tiepolo, 11, I - 34131 Trieste (Italy)

Abstract

In the last years, the Charge Coupled Device (CCD) detectors have had a great development: 2048 × 2048 pixel formats are routinely produced by silicon foundries with good electro-optical characteristics.

Scientific CCDs now, not only offer the ability to be read from more than one output, but they can also be *buttable* to form mosaics in order to cover a larger field of view, requirement posed by the current telescope technology.

The Italian National Telescope GALILEO (TNG) will support a large set of visual and near IR detectors dedicated to scientific measurements at the focal plane. Also tracking systems and Shack-Hartmann wavefront analyzers will be based on CCD technology.

Due to the number of camera systems to be routinely operated, the possibility to have uniformed interaction and configuration of systems is emerged as an important requirement for this crucial part of the telescope.

In this paper the detector and instrument plan foreseen for the TNG telescope will be presented on the first part, while on the second we will present the CCD controller, now at the end of development.

Here presented is a modular system based on digital signal processors (DSP) and transputer modules (TRAM). It is interfaced to host computers (PCs, workstations or VME crates) via optical fibres and a specially developed VME-VSB interface board.

INTRODUCTION

TNG belongs to a new generation of intermediate size telescopes (3.5 meters primary mirror) constructed with the aim to optimize, at the best, the operating conditions of the scientific instrumentation (Ref.1).

It will be operated at the Roque de Los Muchachos Observatory (ORM Canary Islands). The telescope *first-light* is foreseen for the second half of 96, while the instrumentation *first-light* is foreseen for the second quarter of 97, when the first instrument *field-derotator* will be available at one of the two *Nasmyth* focal stations.

As most of the new generation telescopes (ESO's NTT, JNLT among them) the routine operation requires, not only CCD based scientific instrumentation, but also a series of CCD based

CCD MODEL:	MOSAIC:	OUTPUTS:	PIXEL:	PIXELNUM:	SCALE:	FIELD:
LORAL 3EDGE	2×2	8	15 μ	4096×4096	0.08	5.4×5.4
EEV CCD42	1×2	4	13.5 μ	4096×4096	0.07	4.8×4.8
EEV CCD42	2×4	16	13.5 μ	8192×8192	0.07	9.6×9.6

Table 1: Mosaic focal planes for the visual imager.

ancillary instruments for the correct assessment of the overall system. Among them, of particular importance, are the tracking cameras for telescope guidance and the *Shack-Hartmann* (SH) analyzers for telescope optics tuning (active optics). These cameras can look at the focal plane through movable optical probes placed on the instrument derotators.

1. THE TNG INSTRUMENT PLAN

The instrument baseline for the TNG telescope is here briefly reported (see Ref.2 and 3):

- the visual optical imager (OIG) with a minimum covered field of view (FOV) of 5×5 *arcmin*,
- the low dispersion spectrograph (LDS) with resolving power of 1500 and 3500 (echelle mode), and a slit length of 10 *arcmin*,
- the high resolution spectrograph (SARG), with two output cameras giving a maximum resolving power of 50000 and 200000 respectively,
- the infrared imager and spectrograph (NICS) with a 1024×1024 NICMOS array able to work in the wavelength range 0.9-2.5 μm with a maximum covered field of 4×4 *arcmin* and a maximum resolution of 0.125 *arcsec/pixel*,
- the adaptive optics module able to work with an 8×8 *subpupil* system (possible upgrade to 16×16) and coupled to the NICS and OIG instruments.

The first instruments to be available will be the OIG and NICS cameras; they will be both mounted at the Nasmyth station A of TNG. The two spectrographs (to be mounted at the Nasmyth station B) and the adaptive optics module will be ready later.

1.1 DETECTORS FOR THE SCIENTIFIC INSTRUMENTATION

Concerning the optical imager, the present frame of work is to deliver two cameras, both based on a CCD mosaic, for the instrumental *first-light* with the main specifications shown on the first two lines of Tab.1. In this table *scale* is defined in *arcseconds/pixel* while the covered field is defined in *arcminutes*.

The first camera will be based on chips thinned by Steward Obs. and *back-side* treated with the *flash-gate* technology (Ref.4). A batch of $2k \times 2k$ *three edge buttable* chips, made with the SAO design, have been already obtained from LORAL (US) and 5 chips have been commissioned for thinning.

The same batch of chips will cover also the needs of the low resolution spectrograph specifically designed around this kind of chip, and those of the high resolution spectrograph.

The second imaging camera will be based on a mosaic made by two EEV42 chips now under manufacturing at EEV (GB); they will be thinned and *back-side* treated with ion-implantation technology directly at the foundry. Delivery of the chips is expected for the first half of 96. A comparison between the two solutions is shown in Fig.1 and 2, the amount of dead space is about 520 μm (I.E. 40 pixels) in the EEV case and about 400 μm in the Loral case. Fig.1, 2 and 3 are in the same scale.

A third option (see Fig.3), based again on EEV42 chips, but made by 2 \times 4 chips, will be examined after the evaluation of the first EEV camera. This camera will nearly cover all the field available at the telescope adapter-derotator and will pose considerable problems for the provision of the large area photometric filters and for the shutter system.

It should be noticed that all the three cameras will need cryostat windows shaped in a way to correct the field curvature which is typical of *Ritchey-Chretien* telescopes.

1.2 DETECTORS FOR THE TRACKING AND SH SYSTEMS

The main requirements for the tracking cameras are:

- to have good sensitivity,
- to provide good centroiding accuracy,
- to cover enough FOV independently of probe movement,
- to allow short exposures (about 10 mSec) on a small region of interest.

The first two requirements are valid also for the SH case when considering a single spot in place of the tracking star. They are correlated in that, for a given CCD, limiting magnitude and centroiding accuracy both depends on PSF sampling. This can be shown in Fig.4 where the behaviour of centroiding accuracy is plotted versus PSF FWHM for various star magnitudes. PSF is defined in *arcseconds*, accuracy is in pixel fraction, noise, QE and pixel size are those of an EEV05-20 CCD. Telescope parameters are those of TNG, exposure time is 1 *sec* and the equivalent sky brightness is 21 *mag/arcsec*².

The last requirement is mainly intended in order to provide a suitable driving input to the *tip-tilt* tertiary mirror mounted in TNG (maximum frequency of work 20 Hz). This operational frame speed imposes the use of CCDs with half-frame shift capabilities.

From simple geometrical optics it can be shown that the scale (*arcsec/mm*) made at the detector surface for a simple collimator plus camera optics is:

$$S_{scale} = \frac{F_c}{F_t F_{cam} 4.8 \times 10^{-6}} \quad (1)$$

Where $F_c=38500$ *mm* is the telescope combined focal length, $F_t= 510$ *mm* is the collimator focal length and, $f_{cam}=200$ *mm* is the camera focal length. With such conditions (Ref.5) and using an EEV CCD05-20 (770 \times 576 pixels, pixel size 22.5 μmeters) chip we have a scale of 0.3 *arcsec/pixel* and a covered field of about 4 \times 3 *arcmin* when working in *half-frame* mode.

The SH analyzer will collect the light at the same probe as for the tracking camera and the same kind of CCD chip will be used. Two modes of operation are foreseen:

parameter	10 × 10	25 × 25
focal length F_l	84.8 mm	33.9 mm
lenses diameter D_l	1.15 mm	460 μm

Table 2: Main design parameters for SH analyzers.

Mode	10 × 10	25 × 25
TILT	7.35 μm	2.95 μm
DEF	14.7 μm	5.9 μm
4AST	29.4 μm	11.8 μm

Table 3: SH sensitivity to different distortion orders.

- a 25 × 25 sub-pupil SH analyzer,
- a 10 × 10 sub-pupil SH analyzer.

the first one is intended for high accuracy operation while the second is for maximum sensitivity (about 2 magnitudes of gain); mode switching will be obtained moving the optics in front to the CCD.

The optical configuration of this system is shown in Fig.5. In the most general case one can have some optics in front to the SH lenslets array in order to match the collimated beam size D_c to the array size (demagnification factor M_c) and, the same, in front to the detector (demagnification factor M_l) in order to match the CCD size. In practice, being the sensitivity an important factor, one should want to avoid the presence of extra optics in front to the CCD. Moreover some parameters, like F_c and D_c , are fixed by mechanical constraints (SH camera and tracking camera have to work on the same probe) and there is limited freedom on the choice of parameters for SH lenslets. In such conditions the final displacement of one SH spot projected on the CCD surface as a function of the wavefront distortion W , expressed as a local derivative (or local *tilt* on the telescope pupil), is:

$$S_{displ} = M_l \frac{F_l}{N_l D_l} \frac{dW}{dR} \quad (2)$$

where F_l , N_l and D_l are the focal length, the one-dimension number of SH lenses and the single SH lens diameter respectively; R is the radial direction taken on the telescope pupil. So if M_l is forced to one and the pupil matches the lenslets size ($N_l \times D_l$), we can play only with the lenslet focal length F_l .

The optimization of equation 2 in the TNG case, considering the use of a CCD05-20, gives a value of about 4 for M_c and the parameter values shown in Tab.2 for the two modes considered (Ref.6).

Here we made the assumption to sample the Airy pattern, produced by SH lenses under good and/or short integration time, with 2×2 CCD pixels at 500nm. The resulting sensitivity of the analyzer (in terms of spot motion on the CCD detector) to different distortion orders (1λ @ 500nm) is reported in Tab.3.

1.2 DETECTORS FOR THE ADAPTIVE OPTICS SH ANALYZER

All the considerations made in the precedent paragraph for the SH analyzer to be used on the *active-optics* (AOPT) system of TNG are valid also for the *adaptive-optics* (ADOPT) module. The main distinctions are here summarized:

- the ADOPT analyzer will work at short frame periods compared to the AOPT system (some *mSec* compared to tens of *Sec*),
- the ADOPT analyzer will work with a small number of subpupils compared to the AOPT system (5×5 up to 16×16 compared to 10×10 up to 40×40).

The frame rate imposed by the ADOPT system imposes the requirement to have the minimum of readout-noise and the best sampling of SH spots PSF in order to peak the overall sensitivity (see Fig.4). As a result CCD chips for ADOPT purposes are characterized by very small number of pixels (64×64 is a typical case), very high gain output stage and SH spots are sampled directly at the center of four neighbours pixels (macro quadrant cells). EEV is producing under contract a special CCD for this application with parameters shown in Fig.6. The chip, named EEV39, will be processed for quantum efficiency (QE) enhancement and delivered with the EEV42 chips. It is predicted to have a noise of less than 5 electrons up to 1 Mhz pixel rate and less than 2 electrons with optimized sampling time.

The macro cell readout mode is obtained using extensively the horizontal and vertical binning capabilities of the CCD; one example is shown in Fig.7 where the four quadrants (named 1, 2, 3 and 4) are obtained with 2×2 pixel bins, during the same readout also macro pixels A, B, C, D, E and F can be read in order to have a precise estimate of the pedestal for each quadrant. In this example a total of 10 readouts (I.E. ADC conversions), composed by 6 vertical and 24 horizontal shifts are required in order to complete a macro cell scan.

The detector controller sequencer must provide enough flexibility in order to accommodate such kind of readout.

2 THE UNIVERSAL CAMERA CONTROL SYSTEM

In reason of the number of CCD cameras required by the TNG telescope and, in particular, of the need to handle different kinds of detectors for different applications, it has been required to construct a reconfigurable detector controller.

The design of the controller strictly follows the architecture shown in Ref.7. We have made the choice to use transputer processors for data and command handling, taking advantage from the flexible networking and communication scheme provided by this category of processors (see Ref.8, 9 and 10), while, for the task of generating fast and synchronous waveform (*sequencing*) our choice was to use a dedicated DSP (Motorola DSP56001).

The requirement to handle relatively large mosaics of CCD chips has been resolved allowing the insertion of extra analog modules (up to a virtual maximum of 15) driven by the same sequencer module. This choice, of course, makes indispensable the presence of a dedicated *bus*.

In our case we decided to make use of two standard VME P1 backplanes (see Ref.11) redefining the functions of bus lines. This turned out in a great simplification avoiding the costly solution to build a specific bus. In fact the commercial VME P1 backplanes is provided with very good shielding, good power lines and also daisy chains (*interrupt* request lines) that can be used for transputer links wiring. The size of boards constructed is also the standard VME double size format which, when filled with *surface-mount* devices, provides enough space.

The insertion of extra analog modules is facilitated by the presence of transputers links, being data and command handling embedded on the transputer net.

All the boards designed are now available from a commercial company both as spare boards or as a complete system.

2.1 THE DIGITAL SECTION

The overall controller is made of two main sections:

1. the server and adapter module based on the VME-VSB board ATX260,
2. the remote controller based on the slave sequencer board (CCDSEQ) and the slave CCD controller board (CCDCTRL).

Fig.8 shows the splitting between the two parts and the interconnection net between the transputers mounted on each board. The main data link between the two sections is based on the commercial fiber-optic link adapter named TTM27 from Transtech (GB), it allows a data throughput of about 1 Mbyte per second at a maximum communication distance of 1 Km.

The computer control system of TNG is based on a network of distributed VME crates dedicated to low level functions and a number of work-stations for higher level operations. Work-stations can be also equipped with a VME bus subsystem (HP747). In order to be fully compliant with the above standards the CCD controller must present, to the external world, a VME interface. In the ATX260 case this is obtained communicating via the VSB auxiliary bus with a commercial bank of dual-ported (VME-VSB) memory.

This choice allows the direct commanding and collection of data from the workstation in asynchronous way, moreover the entire scientific frame is fully buffered on the dual-ported memory. If required it is also possible to mount the boards on a more standard VME crate with a dedicated master CPU for data communication through standard communication network (ETHERNET, FDDI etc.).

2.1.1 THE SEQUENCER

The CCDSEQ board is shown in Fig.10, one can see the main features of the board:

- a T225 transputer for command and data exchange,
- a CCD state sequencer based on a DSP Motorola 56001 booted from the T225,
- a shutter timer handled by the DSP (24 bits, 0.5 *mSec* resolution),
- a 6 channels temperature multiplexer with 12 bits ADC handled by the DSP,
- an ON-OFF temperature controller with 12 bits DAC for detector temperature setting.

The choice to use a dedicated DSP as sequencer (Ref.11) in place of other solutions like ring memory buffers (Ref.12) has been made because it gives the best compromise between speed attainable and simplicity of the microcode involved.

In our case the DSP56K is part of a commercial TRAM module (DTM560 from Perimos, Germany) mounting also a T225 transputer processor memory coupled to it.

The DSP generates sequences of waveform making use of two memory mapped ports available on the controller bus; the two ports are made one, STA, by 16 lines while the second, STB, is made by 12 lines. They can be directly used from other boards mounted on the bus in order to generate CCD clock pulses or for internal timing functions.

The DSP directly writes the required status on STA or STB (usually STA is used for serial CCD timing while, STB, is used for parallel CCD timing) taking the data from tables previously loaded in memory. Each table entry (24 bits) is made by the output status (16 LS bits) and the number of wait states associated with it (8 MS bits).

Operating the DSP sequencer in this way it is possible to have a minimum pulse width on the output ports of 100 *nsec* which is maintained all along the working table; of course there is the insertion of an extra delay (600 *nSec*), due to looping instructions, every time the table finishes and restarts for a new pixel. In practice the minimum pixel time is limited by this extra delay.

In the case of time critical applications (adaptive optics) one should want to work without any pixel to pixel interposed delay; taking advantage of the very limited size of chips used for such applications (not more than 40 pixels per output) it is possible to cover the entire stream of horizontal pixels with a single waveform table avoiding any extra delay in-between pixels but only at every line end.

For large format chips the typical way to do a full CCD readout is to split it in loops of table-driven *microscans* (I.E. a one line parallel shift, a one pixel serial shift at right, the same at left, etc.).

The overall performance attainable is well aligned with the rest of the hardware, in particular, the switching speed of the clock drivers (CMOS switches) matches the 100 *nSec* minimum pulse time available. The sequencer has been proved to be satisfactory also with the clocking scheme of several IR detectors (Ref.13 and 14).

2.1.2 THE TRANSPUTER ADAPTER BOARD

This card, called ATX260, has been commissioned to a private company (ATENIX Italy) and is shown in Fig.9. It is a double bus board (VME A16 and VSB A32), where the CPU (a T805 transputer) can directly address a VSB interface and, through the four data communication links, can handle a network of slave transputers.

One link is directly mapped on the VME bus in order to allow the network boot and debugging from the host computer, the other three links can be patched to two size2 and one size4 TRAM site. It is also possible to interrupt or reset the T805 from the VME bus.

In the typical configuration the size4 TRAM site mounts a commercial graphics module (in our case the TTG3 from Transtech) for real-time display of CCD data.

It has been demonstrated the T805 transputer, due to its transfer speed (about 40 *Mbytes/Sec* of transfer speed to the external bus) and bus flexibility, is a nearly perfect DMA engine. The resulting data transfer speed on the VSB bus is on the order of 6-8 *Mbytes/Sec* (limited by the dual-ported memory speed); a programmable gate array (PGA) logic takes care of byte and word swapping on the fly.

The commanding of the board and its associated network is made, as for data transfers, using a block of dedicated shareable area on the VME/VSB memory and the T805 interrupt line mapped on the VME bus. A simple, *widget* based, command interface has been made directly inside the commercial data processing software called IDL (RSI, US). This allow, through the use of a VME driver linked with IDL, the instrument commanding, the data collection and data analysis on the same ambient.

2.2 THE ANALOG SECTION

The analog section, with the only exception of the 4× channels preamplifier board and the power-supply board, is entirely mounted on the CCDCTRL board. This board has been commissioned to a private company (LES Italy). One single CCDCTRL board can drive one 4× outputs CCD chip or a small 2×2 CCD mosaic making use of one output per chip. All the internal functions are managed by a T225 transputer coupled to a XILINX PGA.

Multiple boards can be inserted extending the transputer net through the backplane. The functions covered by the board are shown in Fig.11 and here summarized:

- 4× correlated double samplers (CDS) channels,
- 4× 16 bits ADCs (CRYSTAL) used for CDS and telemetry service,
- 4× 18 bits DACs for off-set programming inside CDS channels,
- 16× CCD clocks drivers with independently programmable upper and lower levels (8 bits DACs),
- 8× CCD bias drivers with independently programmable levels (12 bits DACs),
- 24× telemetry channels (16 bits) placed on CCD clocks and bias.

All the converter used inside the board are with serial input or output in a way to avoid the need to carry along the board a data bus. The printed circuit requires 8 layers, of which, two are used as digital and analog shield. Looking at Fig.11 one can see the lines denominated DA_DATA, DA_CLOCK and some *chip-select* wires allowing the programming of all the DACs mounted on the board. Data serialization and parallelization for DACs and ADCs is made *on the-fly* by the PGA reducing at the minimum the transputer intervent.

The analog processing chain is made by four independent channels, one of them is shown in Fig.12. This is the typical configuration with differential preamplifier, line-clamp, CDS and conversion. Particular care has been dedicated to the choice of the ramp inverter in front to the integrator. A difference of gain magnitude in the two conditions (normal, reversed) can create some non-linear behaviour in the CDS output; we found that the best solution is to switch directly in front of an instrumental OPamp.

The minimum CDS pixel time is limited by the Crystal ADC at about 10 μ Sec.

5. CONCLUSIONS

The instrument plan for the TNG telescope is in a well advanced stage of implementation. In particular the CCD detector purchasing plan is already started and will terminate in the middle of 96. The detector controller plan is going towards the conclusion; all parts have been implemented and tested. We expect to provide the preliminary set of scientific and auxiliary detector systems in schedule with the telescope construction.

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Fig.1, 2, 3 CCD mosaic focal planes.

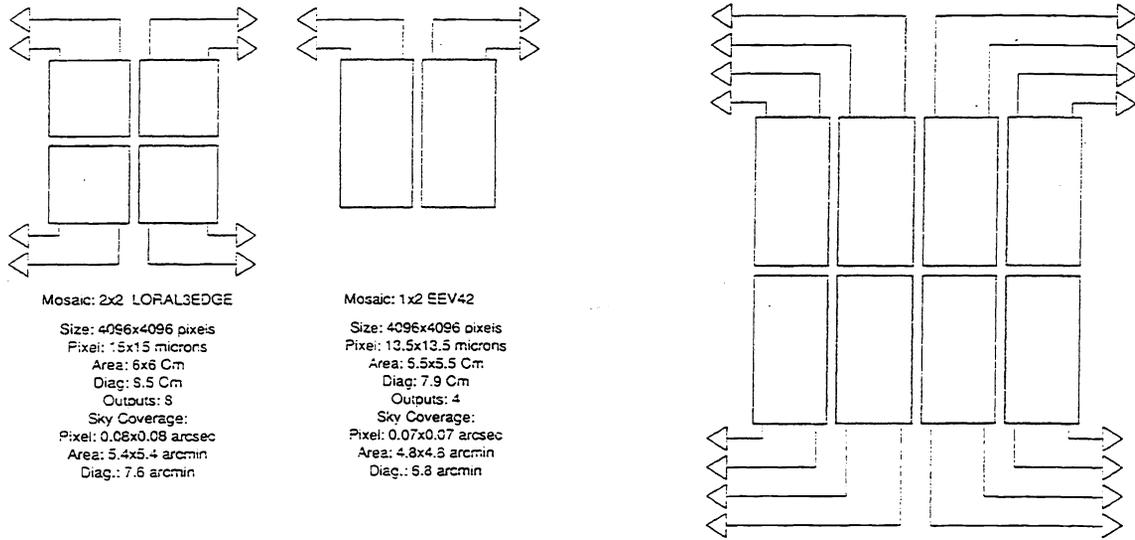


Fig.4, Tracker sensitivity.

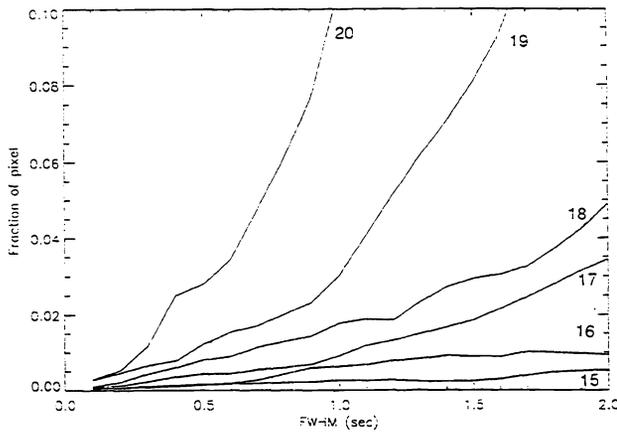


Fig.5, SH camera optics.

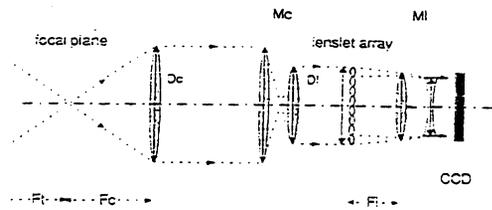


Fig.8, CCD controller transputer net.

Fig.6, CCD EEV39. Fig.7, Quadrant cell.

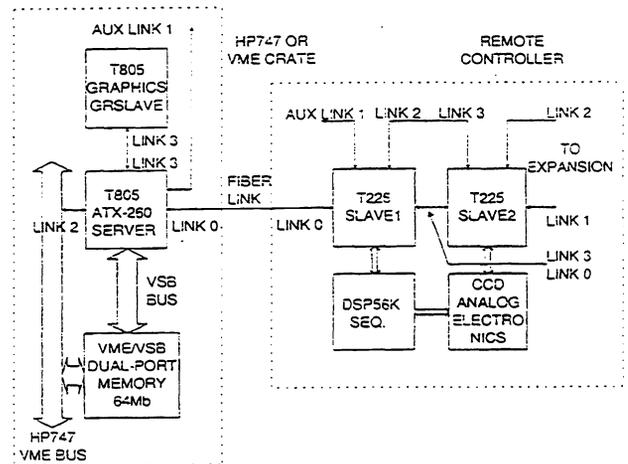
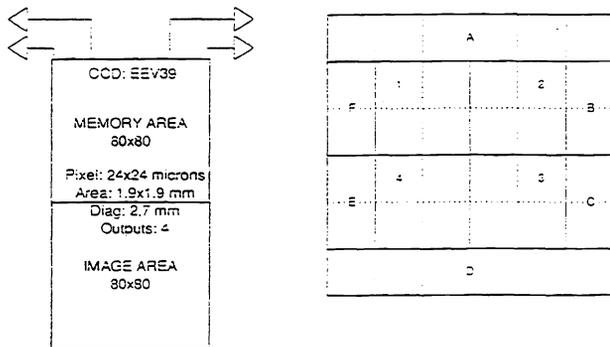


Fig.9, ATX260 transputer adapter board.

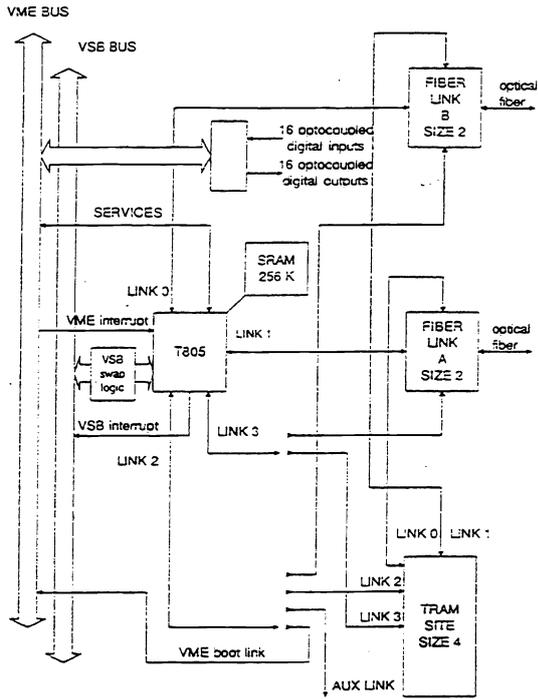


Fig.10, CCD sequencer board.

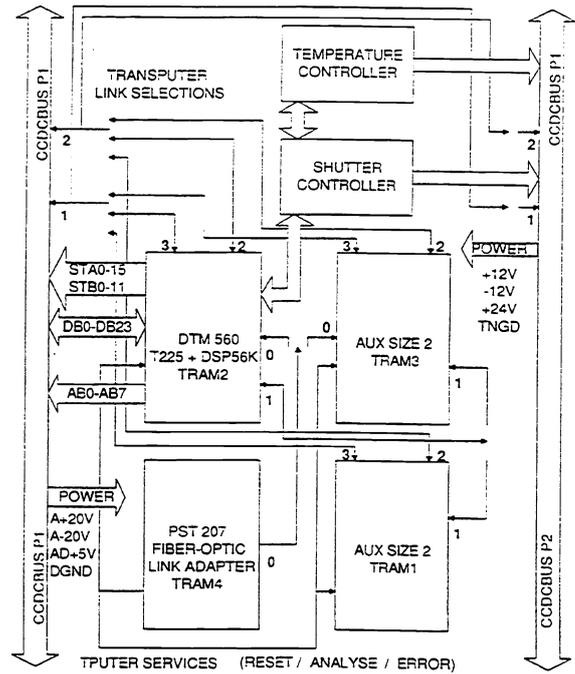


Fig.11, CCD controller board.

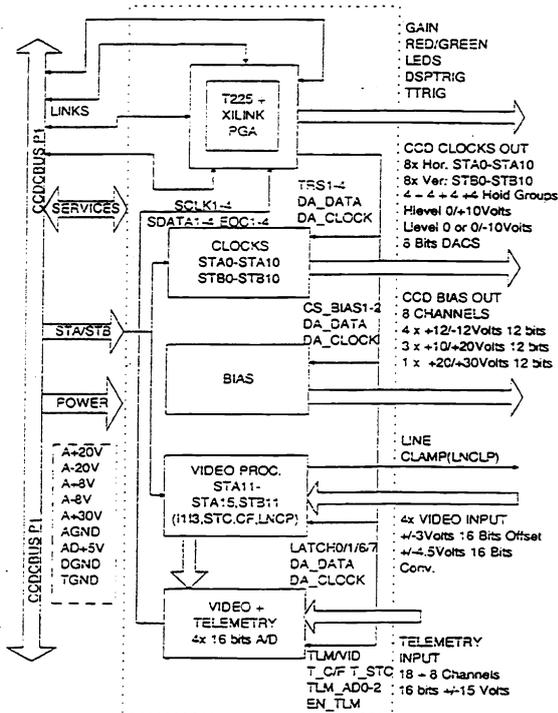


Fig.12, CCD video processing pipe-line.

