Possibilistic Worst Case Distance and applications to circuit sizing

Eva Sciacca[1], Salvatore Spinella[2], and Angelo Marcello Anile[1]

[1] Dipartimento di Matematica e Informatica,
Università degli studi di Catania, Viale A. Doria 6, I 95125 Catania, Italy
sciacca@dmi.unict.it
[2] Consorzio Catania Ricerche, via A. Sangiuliano 262,
I 95124 Catania, Italy
spins@unical.it

Abstract. The optimization methodology proposed in this work is inspired to [1] and is named Possibilistic Worst-Case Distance (PWCD). This scheme has been tested on an application related to the MOS device sizing of a two stage Operational Transconductance Amplifier circuit (OTA) [2]. In order to model the uncertainties arising from circuit parameter simulations the fuzzy set theory, introduced by Zadeh [3], has been used. A linearization of the circuit performances as function of circuit parameters has been fitted as suitable approximation in a finite range, this choice was suggested to reduce the computational cost related to simulations of the real design. By means of linearization the circuit performances were fuzzyfied and a possibility measure of performance failure was minimized. The proposed case study will show that the possibilistic approach to the worst case analysis, even though less accurate for indirect yield estimation with respect to the probabilistic one, can identify an optimal design in yield terms. Furthermore the possibilistic methodology allows to develop calculation without any statistical hypothesis or sensitive analysis.

1. Introduction

The new technologies of MOS with shrinking dimensions have accelerated in the last decade and most likely they point at a typical dimension significantly lower than 80-100 nm in the next few years. Under 80-100 nm the process variations start to build-up and have a sizable effect on circuit's performances. Therefore the exploration of advanced circuits design is mandatory in order to anticipate the challenge of future behaviour of circuit based on nanoscale CMOS devices. Examples of these challenges are parasitic, process variation and transistor reliability. It is necessary to have models for MOS devices able to predict accurately new physical effects arising from this miniaturization and easy to integrate into simulation flow.

2. Worst Case Analysis and Possibility

The analysis of the *worst case* scenario is a fundamental step of any design process [4, 5]. The worst case of a manufacturing process is the failure of a performance specification in the inspection test after manufacturing. In order to prevent this event, many simulations are carried out on the design to increase the manufacturing yield [5]. The computational cost of these simulations are very high because they simulate statistically process variations and increase the yield asymptotically with respect to a random process or deduce an indirect measure for the yield through statistical assumptions [6].

One assumes a simulation process involves:

- **controllable design parameters $\mathbf{X_c}$**, which is possible to define in reliable way with respect to the manufacturing process, for instance the geometrical structure of a device;
- **uncontrollable model parameters $\mathbf{X_u}$**, which are known in terms of confidence interval for the simulated model, their values are fit from experimental data for each technology node and then fixed over a range of process variations;
- **operational parameter $\mathbf{X_o}$**, which are operational range where the performances must be maintained, for instance the temperature or the power supply.

With respect to these classes of parameters the performances can be defined in functional terms as:

$$P = y(X_c, X_u, X_o) \tag{1}$$

The uncertainty concerning the uncontrolled parameters and the necessity to cover a wide range of operational parameters compel to consider these parameters as fuzzy numbers and to interpret the previous formulation as:

$$\widetilde{P} = \widetilde{y}(X_c, \widetilde{X}_u, \widetilde{X}_o) \tag{2}$$

where $\widetilde{P}$ is the fuzzy representation of the performances and only the controllable parameters are considered crisp.

In order to deal with design specifications it is necessary to compare the fuzzy numbers representing the performances with crisp numbers representing the design constraints and give a measure of satisfaction of these constraints. For this purpose the possibility measure of failure with respect to the specification constraints can give useful information to improve the yield and design [7]. Note that a fuzzy number may also be considered as the trace of a possibility measure Π on the singletons (single elements) x of the universal set X. When a possibility measure is considered, its possibility distribution π is then interpreted as the membership function of a fuzzy number $\widetilde{B}$ describing the event that Π focuses on, as follows:

$$\Pi(\{x\}) = \pi(x) = \widetilde{B}(x), \qquad \forall x \in X \tag{3}$$

The possibility measure of a crisp number being smaller or equal to a fuzzy number B is then defined as follows [8]:

$$\Pi_{\widetilde{B}}([x,+\infty)) = \sup_{y \geq x} \widetilde{B}(y), \qquad \forall x \tag{4}$$

Based on 3 and 4, given a representation of the performance P and maximal failure specification performance P_f then the possibility measure of failure of this performance is a measure for the event $P > P_f$, hence

$$\Pi_{\widetilde{P}-P_f}([0,+\infty)) = \sup_{y \geq 0} (\widetilde{P} - P_f)(y), \qquad \forall x \tag{5}$$

From possibility measures of all performance failures it is possible to deduce a vector of measures ($p_1, \ldots ,p_n$) for a given design. A metric L_n can summarize all of them and it is used as target of the optimization process, for instance $n = 2$ represents the Euclidian norm.

3. Fuzzyfication through linearization and sampling

In order to model with fuzzy numbers the uncertainty arising from simulation design a linearization of the performance can be used as suitable approximation. The linearization is fitted with respect to the uncertain parameters (uncontrollable and operational) to give an estimation of the behaviour of the performance as function of them. The scheme is the following

$$\overline{P} = \overline{Y}_{X_c}(X_u, X_o) = q + X_u \cdot A_u + X_o \cdot A_o \tag{6}$$

where the linearization $\overline{Y}$ of the performance P is carried out as linear function of $\boldsymbol{X_u}$ and $\boldsymbol{X_o}$ in a finite parameter range. The linearization coefficients represented in the vectors $\boldsymbol{A_u}$, $\boldsymbol{A_o}$ and the constant q are computed through a latin hyper-cube sampling in order to reduce the number of samples in a N-dimensional sparse space. This sampling scheme generates a multidimensional distribution of parameters where there is only one sample in each line parallel to the axes. Notice that these kinds of rough analysis are often used in circuit design.

From this linearization, the fuzzyfication is carried out using a uniform random sampling on the parameter ranges and giving a fuzzy representation of the linearized performance enveloping its sampling by interval. The fuzzy map is constructed by α-level considering the minimum median interval which envelops a fraction (1- α) of the linearized performance [9].

The possibilistic worst-case parameter sets for all specifications determine the worst-case behaviour with an accuracy according to the underlying method for performance evaluation, i.e., exactly when using numerical simulation or approximately when using performance macromodeling techniques.

4. The OTA

The BSIM model card involved in circuit simulation has hundred of parameters to characterize the I-V curve of a MOSFET device, but only a tens of them are critical and determine the technology scaling design. In particular the channel length (L_{eff}), the oxide capacity (T_{ox}), the threshold tension (V_{th0}), and the drain source resistance (R_{dsw}) are essential to characterize the technology process [10]. Hence the uncertainty of these parameters must be taken into account in order to determine the optimal device sizing to reach good performances in a technology scaling.

The computational cost related to the statistical representation of the technology parameters requires a methodology to reduce the number of simulations. Furthermore a design methodology should avoid to point deterministically towards unfeasible over-designs because this could have the opposite effect blocking the optimization process at initial stages. The previous linearization and fuzzyfication was found useful for that purpose.

Table 1. OTA parameters: type, ranges, unit

Parameter	Type	Ranges	Unit
temp	Operational	0 - 50	*Degree*
V_{V1}	Operational	3.5 – 4.2	*V*
L_{eff}	Technological	0.9 ± *perc*	*μm*
NMOS T_{ox}	Technological	9. ± *perc*	*nm*
NMOS V_{th0}	Technological	0.6322 ± *perc*	*V*
NMOS R_{dsw}	Technological	650 ± *perc*	*ohm · μm*
PMOS T_{ox}	Technological	9. ± *perc*	*nm*
PMOS V_{th0}	Technological	-0.6733 ± *perc*	*V*
PMOS R_{dsw}	Technological	460 ± *perc*	*ohm · μm*
$W_{1b}= W_{1a}$	Geometrical	0.6 – 20	*μm*
W_3	Geometrical	0.6 – 20	*μm*
W_5	Geometrical	0.6 – 20	*μm*
W_4	Geometrical	0.6 – 20	*μm*
$W_{2b}= W_{2a}$	Geometrical	0.6 – 20	*μm*
C	Geometrical	1 – 15	*pF*
R	Geometrical	2- 40	*KΩ*

Formally, let **W**, *C* and *R* be the design parameters respectively the MOSFET widths, the capacity and the resistance of the compensation net. Let **o** be the operational parameters (temperature *temp* and supply voltage V_{V1}). And let **t** be the process parameters (L_{eff}, T_{ox},V_{th0}, R_{dsw}). The uncertainty of process parameters is expressed as percentage of a reference value [11] and it defines a range of uncertainty. Tested values are ± 3%, ± 5%, and ± 7%. Table 1 shows the ranges which envelope the uncertainty of process and operational parameters and ranges for geometrical design parameters.

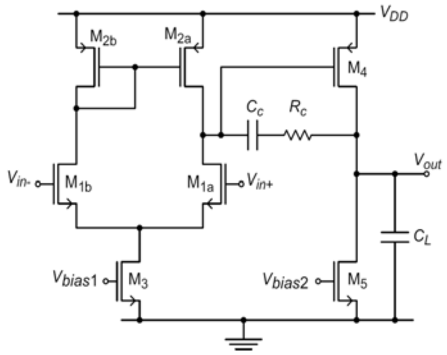


Fig. 1 Two stage OTA net topology.

The figure 1 shows the circuit net of the two stage OTA [2]. Some of the main performances of this very useful electronic component are:

- **Gain@100Hz**,which is the base gain of the amplification;
- **Phase margin**, which is related to the circuit stability and to the parasitic effects like cross coupling (the main reason of circuit failure);
- **Unity gain frequency**, defined as the frequency value where the gain is equal to one;
- **Power dissipation,** which is a very important performance for all devices supplied by batteries.

The circuit performances represented by a vector *P* are computed by simulation *Y*

$$P = Y(w,t,o) \qquad (7)$$

where

- *w* represent the geometrical parameters of the MOSFET devices and RC components of the net (*controllable*),
- *t* represent the uncertain technological parameters related to the manufacturing (*uncontrollable*),
- *o* represent the operational parameters whose range must be covered with acceptable performances (*operational*).

Therefore it is possible to proceed with linearization and fuzzyfication introduced in the previous section in order to obtain a fuzzy vector representing the performances of a given OTA circuit based on specific sizing defined by controllable parameters. It is possible to define a functional operator *Linearize* as:

$$a = Linearize_w(Y, I_o, I_t) \tag{8}$$

where I_o (operational) and I_t (technological) are the intervals defined in table 1 by ranges. The fuzzyfication is then carried out by sampling and building the median interval as described in the previous section.

5. PWCD pseudo-code

The following pseudo-code explains the main functionality of the Possibilistic Worst-Case Distance methodology, that is the procedure which computes the optimization function to be minimized by the Simplex method with Simulated Annealing [12]:

FuzzyCircuitFun(**w**, $\boldsymbol{inf_{t,o}}$, $\boldsymbol{sup_{t,o}}$)

1. coefficients:= *LinearizeFun*(**w**, $\boldsymbol{inf_{t,o}}$, $\boldsymbol{sup_{t,o}}$, *CircuitFun*)
2. r:= random variables between $\boldsymbol{inf_{t,o}}$ and $\boldsymbol{sup_{t,o}}$ uniformly generated
3. $\tilde{P}$:=*FuzzyfyFun* (coefficients, r)
4. Calculate the measures of possibility of failure given $\tilde{P}$ and P_{fi}
5. Get the sum of the failure possibility measures.

- *LinearizeFun* is the procedure which implements the linearization operator of the circuit performance responses (see equation 8).
- *LatinizeFun* computes latin hyper-cube sampling with a number of points twice as parameter dimensions.
- *FuzzyfyFun* computes the fuzzyfied circuit performance $\hat{P}$ by equation 2.
- *CircuitFun* is the function to interface the circuit simulator (see equation 7).

6. Results

The test carried out is aimed to guarantee the specification performances with an optimal choice of the geometrical parameters taking into account the uncertainty of the uncontrollable and operational parameters. An optimization performed with the Possibilistic Worst-Case Distance (PWCD) (see equation 5) on the specification given in table 2.

Table 2. Performance failures for the tested circuit

Performance P	***Failure P_f***	***Unit***
Gain @ 100 Hz	< 60	dB
Phase margin	< 60	Degree
Unity gain frequency	< 20	MHz
Power dissipation	> 0.67	mW

The function to optimize was

$$\sum_{i \in I} \Pi_{(P_i - P_{fi})}([0,+\infty)) \tag{9}$$

where I is the set of performance P_i to guarantee and P_{fi} is the specification failure.

The sum of possibilities is the L_1 norm inside the space of the problem objectives possibilities. This choice allows the characterization of convex regions of the multi-objective problem with a suitable merit function.

The circuit simulator used is Spice in the implementation named *ngspice* [13] with BiSim3 MOSFET model card.

The graphic in figure 2 shows the comparison between Possibilistic Worst-Case Distance methodology and the most common design methodology used in microelectronic industry named “Nominal Over-Design”. It is shown the comparison of the two methodologies in terms of the resultant yield.

The Nominal Over-Design methodology fixes every objective to a secure value with reference to the nominal specifications. In this test case the objectives were increased of a 10% with regard to the minimum thresholds and decreased of a 10% with regard to the maximum thresholds.

Both methodologies used the Nelder-Mead simplex optimization algorithm with Simulated Annealing [14]. The scheduling of annealing temperature allows to coordinate the convergence of optimization variables making global the searching procedure.

A circuit is classified as “acceptable” if every performance specification is satisfied. In the microelectronic industry context, the “yield” is the ratio between acceptable circuits over the whole production of circuits [5]. The yield value was computed by means of Montecarlo simulations. Three independent tests were carried out considering a statistical distribution of the technological parameters of 3%, 5% and 7% with respect to the nominal default value of the model card [11]. Every test executed 2000 simulations.

The graphic in figure 2 shows that Nominal Over-Design methodology (light grey) involves a large variability of yield values. Therefore, this methodology, widely utilized, gives no guarantee of robustness. On the contrary, PWCD methodology (dark grey) shows high values of yield and therefore robust yield results in relation to the considered uncertainty.

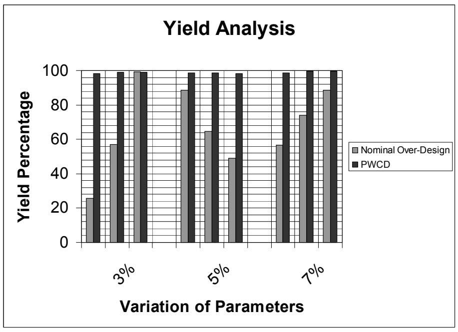
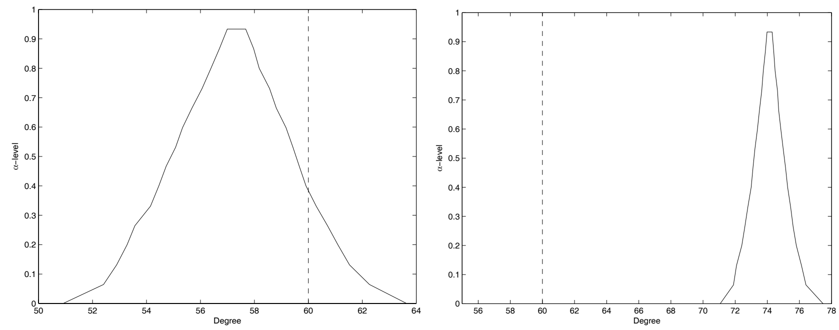


Fig. 2. Yield results of Nominal Over-Design and Possibilistic Worst-Case Distance methodologies carried out by means of Montecarlo simulations.

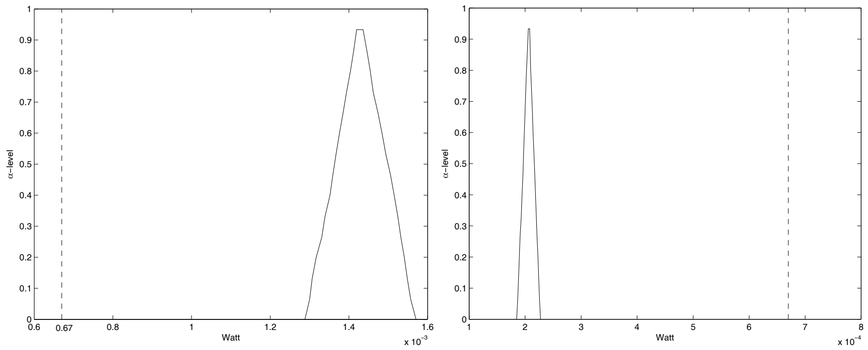
The graphics in figure 3 show the fuzzy numbers of the circuit performances *Phase margin* and *Power dissipation* as against the failure specification shown in table 2. Graphics on the left side show these fuzzy numbers before optimization on initialization step of the simplex optimization algorithm, while graphics on the right side show fuzzy numbers of the circuit performances after the optimization process.

This typology of electronic design takes into account the trade-off between different objectives during searching of the optimal design. In general, given a starting configuration, only few constraints are satisfied. The optimization must find a new configuration to satisfy all constraints simultaneously with a safety margins. The effectiveness of the methodology is shown by the graphics on the right side which point out the constraint satisfaction.

Graphics in figure 4 show the fuzzy numbers representing the performances *Unity Gain Frequency* and *Gain @ 100 Hz* at different technological parameter variations of 5%, 7% and 9%. Notice that the increasing of parameter uncertainties changes the value of the performances and their relative uncertainties.



(a) (b)



(c) (d)

Fig. 3. (a), (b) represent the fuzzy number Phase margin (solid line) with respect to the failure value of 60 *Degree* (dashed line) before (a) and after (b) optimization methodology. (c), (d) represent the fuzzy number Power dissipation (solid line) with respect to the failure value of 0.67 *mW* (dashed line) before (c) and after (d) optimization methodology.

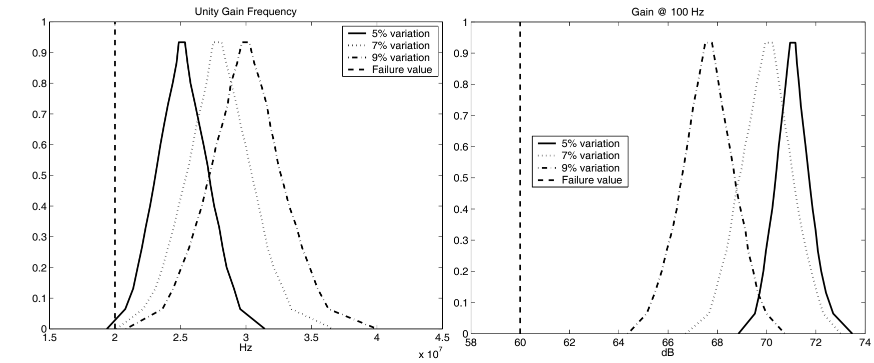


Fig.4. Fuzzy numbers representing the performances Unity Gain Frequency and Gain @ 100 Hz at different technological parameters variations (5%, 7%, 9%).

7. Conclusions

The Possibilistic Worst-Case Distance optimization methodology made use of concepts from fuzzy set and possibilistic theory to model uncertainty of circuit parameters in order to evaluate and to minimize the Worst-Case Distance. Briefly, this methodology showed the following advantages:

- the uncertainty arising from circuit design has been modelled by means of a methodology that avoid statistical hypothesis or sensitive analysis;

- the new optimization methodology has a good behaviour over a wide range of process and design conditions;
- PWCD features are suitable to be integrated into optimization flows. The problem specification of worst-case distance is in accordance with common circuit design problem specifications;
- the methodology made use only of the circuit simulation scheme without any other analysis tools of analog circuits;
- the methodology provides a real approach to reduce the computational effort of a design based on fuzzy set to model uncertainty.

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